FPGA SYSTEM FOR CYCLOTRON RF POWER SUPPLY CONTROL

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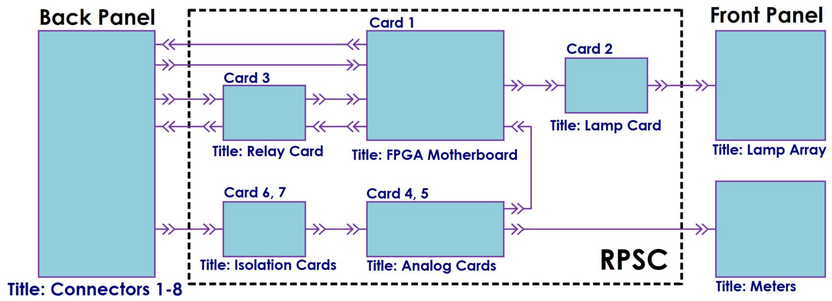
The RF Power Supply Control (RPSC)

- The UW Medical Cyclotron Facility (MCF) features a 50MeV multi-particle accelerator for neutron therapy and cancer research.
- Built in the 1980s, the RPSC handles command, status, and interlock signals for the cyclotron's power supplies.
- Composed of 15 analog, logic, and flip-flop cards.
- Upgrading this system with an FPGA will allow for faster and more reliable control leading to less downtime for repairs.
- Providing documentation for HDL will also enable the MCF team to develop future FPGA designs.

System Overview

Seven PCBs handle the hardware side of the system.

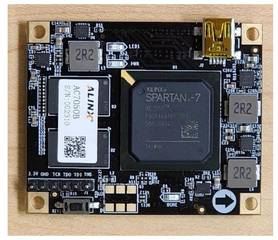
- Motherboard Card: Houses the FPGA and deals with voltage shifting/protection.
- Lamp and Relay Cards: Handles the lamp and relay signals controlled by the FPGA.
- Two Analog Cards: Processes the analog signals of the system.
- Two Isolation Cards: Isolates the power supplies of certain analog signals.



Hardware Design

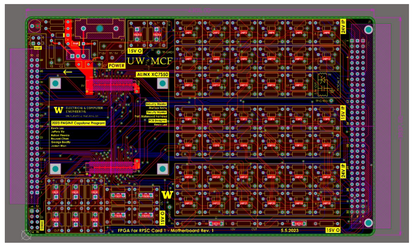
FPGA Selection:

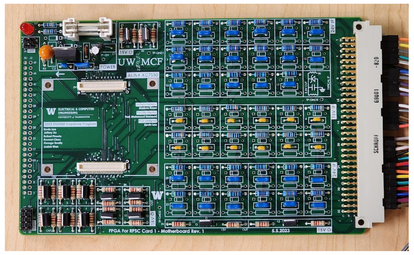
- Xilinx Spartan-7 XC7S50 System on Module (SOM)
- Provides 114 I/O pins for required parallel connections.
- Industrial SOMs are reliable and can be easily replaced without any solder work.



PCB Design:

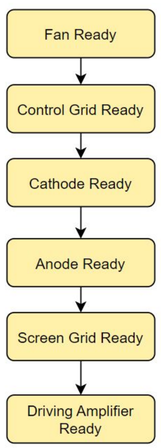
- PCB layouts are organized by circuit types with test points to increase maintainability.
- All cards use through-hole components that are stocked by the facility.
- All cards are connected using the facility's Schroff standard for rack-mounted systems.
- Analog Cards: Power supplies' voltage and current levels pass through a 3-stage op-amp ADC for the FPGA.
- Isolation Cards: Uses isolation amplifiers for voltage reference separation.

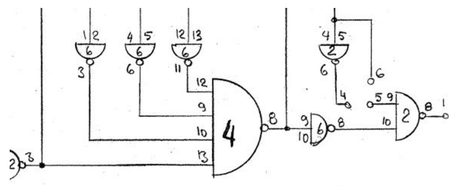




Digital Design

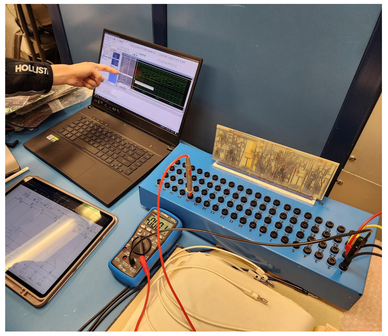
- Existing control logic adapted using HDL.
- Follows cyclotron power supply startup sequence.
- Monitors and flags subsystems for faults.
- Indicates correct function by lighting the assigned lamp on the front panel.
- Replaces analog delay circuits with digital equivalents.
- FPGA connects to a ESP32 ethernet module through UART.
- Potential real time system monitoring with the facility's EPICS ethernet control system.

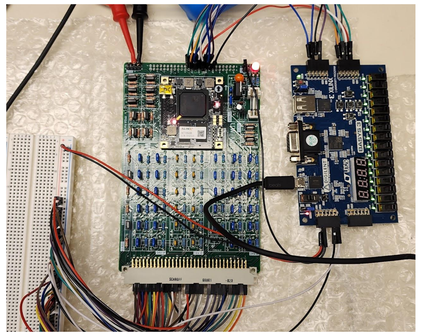




System Validation

- All Verilog modules are simulated with specific fault cases.
- The logic is further validated against existing card behavior.
- Utilize a separate testing FPGA to rapidly verify the overall design.
- Full system input voltage levels (15V and 24V) will be used to test the hardware while using transients to test protection circuitry.





Future Work and Acknowledgments

- Further system functional testing.
- Integrating EPICS control system protocol over ethernet.
- Manufacture new RPSC enclosure.
- Install and test within the overall RF system.
- Develop second identical RPSC for the parallel RF tower.

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